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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PRENTY, MARK V	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,477	YAMAZAKI, SHUNPEI	
	Examiner	Art Unit	
	MARK PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24,25,28-30,33-35,38,39,41,43,44,46,48,49,51 and 53-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39,41,43,44,46,48,49,51,53 and 57-59* is/are allowed.

6)☒ Claim(s) *24,25,28-30,33-35,38 and 54-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the response filed on January 23, 2006.

Claims 24, 25, 28 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,455,791 to Zaleski et al. (Zaleski, already of record) together with United States Patent 6,127,702 to Yamazaki et al. (Yamazaki, already of record). Please note that this rejection has been changed to the extent it now relies more on Yamazaki's Figs. 17A-17C disclosure, as explained below.

With respect to independent claim 24, Zaleski discloses a semiconductor device (see the entire patent, including the Fig. 1 disclosure) comprising: a semiconductor film 2b; a pair of first impurity regions 4a, 4b being formed in the semiconductor film; an active region 4c formed between the pair of first impurity regions in the semiconductor film; a floating gate 6 formed over and insulated from the active region; and a control gate 8 formed over and insulated from the floating gate.

The difference between claim 24 and Zaleski is claim 24 further comprises: "at least two second impurity regions formed in said semiconductor film between the pair of first impurity regions; at least one channel region between the at least two second impurity regions, boundaries between the channel region and the at least two second impurity regions extend in a direction along a carrier flow direction of the channel region...wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions."

Yamazaki teaches providing a thin film transistor with at least two second impurity regions extending from the source region into the drain region in order to

suppress short channel effects, among other things (see the entire patent, particularly Fig. 17C's regions 1709).

It would have been obvious to one skilled in this art to provide Zaleski's thin film transistor with at least two second impurity regions extending from source region 4b into drain region 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least the source region (i.e., "at least one of the pair of the first impurity regions") and the at least two second impurity regions) in order to suppress short channel effects as taught by Yamazaki.

Claim 24 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 25, Yamazaki teaches that its second impurity regions preferably have a striped shape (see Fig. 17C's second impurity regions 1709).

Claim 25 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 28, Yamazaki also teaches that thin film semiconductor devices are conventionally used in electronic devices such as a mobile computer, for example (see Yamazaki's Figs. 20-21 disclosure). It would have been further obvious to one skilled in the art to use the obvious Zaleski/Yamazaki semiconductor device in a mobile computer because Yamazaki further teaches that thin film semiconductor devices are conventionally used in electronic devices such as a mobile computer.

Claim 28 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

With respect to dependent claim 54, Zaleski's device further comprises an insulating layer 3 that underlies semiconductor film 2b, and Yamazaki further teaches that such an insulating layer should comprise the same conductivity type impurity element as the at least two second impurity regions (see the Embodiment 11 disclosure at columns 28-29).

Claim 54 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki.

Claims 29, 30, 33, 34, 35, 38, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 5,455,791 to Zaleski et al. (Zaleski, already of record) together with United States Patent 6,127,702 to Yamazaki et al. (Yamazaki, already of record) and United States Patent 5,814,854 to Liu et al (Liu, already of record).

Independent claim 29 parallels independent claim 24 except that claim 29 further recites a NOR type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki is thus hereby incorporated by reference into this rejection of claim 29 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The difference, therefore, between independent claim 29 and the obvious Zaleski/Yamazaki device is claim 29 recites a NOR type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NOR type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Yamazaki EEPROM device in a NOR type circuit because Liu teaches that EEPROM devices are conventionally used to form a NOR type circuit.

Claim 29 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 29's dependent claims 30 and 33 parallel independent claim 24's dependent claims 25 and 28 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 34 parallels independent claim 24 except that claim 34 further recites a NAND type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki is thus hereby incorporated by reference into this rejection of claim 34 under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

The difference, therefore, between independent claim 34 and the obvious Zaleski/Yamazaki device is claim 29 recites a NAND type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NAND type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Zaleski/Yamazaki EEPROM device in a NAND type circuit because Liu teaches that EEPROM devices are conventionally used to form a NAND type circuit.

Claim 34 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Independent claim 34's dependent claims 35 and 38 parallel independent claim 24's dependent claims 25 and 28 (addressed above) and are thus also rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

With respect to dependent claims 55 and 56, Zaleski's device further comprises an insulating layer 3 that underlies semiconductor film 2b, and Yamazaki further teaches that such an insulating layer should comprise the same conductivity type impurity element as the at least two second impurity regions (see the Embodiment 11 disclosure at columns 28-29).

Claims 55 and 56 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Zaleski together with Yamazaki and Liu.

Claims 39, 41, 43, 44, 46, 48, 49, 51, 53 and 57-59 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable semiconductor devices taken as a whole, including the floating gate.

The applicant's remarks are somewhat moot in view of the change in the rejection, but are addressed below to the extent they might still be relevant.

The applicant's remark: "In particular [with reference to Yamazaki's Fig. 17A], at a boundary between a source region 1702 and the channel region 1704, the edge of the [pinning] region 1701 is aligned with the channel region 1704. In contrast, at a boundary between a drain region 1703 and the channel region 1704, the other edge of the [pinning] region 1701 is not aligned with the channel region 1704," is correct and actually supports the rejection. Specifically, the fact that Yamazaki discloses that its Figs. 17A-17C channel regions and pinning regions are aligned along the source region supports the rejection's premise that: "It would have been obvious to one skilled in this art to provide Zaleski's thin film transistor with at least two second impurity regions extending from source region 4b into drain region 4a (resulting in a semiconductor device whose floating gate overlaps a boundary between at least the source region (i.e., "at least one of the pair of the first impurity regions") and the at least two second impurity regions) in order to suppress short channel effects as taught by Yamazaki."

The applicant's remark: "as explained above in Figs. 17A-17C of Yamazaki, at the boundary between the channel regions and the drain region, the channel regions are not aligned with the pinning region," is correct, but Yamazaki's Fig. 17A-17C channel regions are aligned with the pinning regions along the source region.

The applicant correctly quotes Yamazaki as disclosing: "it is preferred that [Fig. 1A's] impurity regions 104 be formed so as to extend to the inside of the drain region 102. Conversely, it is preferred that the impurity regions 104 be formed so as not to extend to the inside of the source region 101," but the applicant's conclusion: "Therefore, in Fig. 1A in Yamazaki, the [pinning] regions are clearly located apart (not

aligned) from the channel region," is incorrect. Specifically, Yamazaki's disclosure that Fig. 1A's impurity regions 104 are preferably formed "so as not to extend to the inside of the source region 101," does not mean that the impurity regions 104 "are clearly located apart (not aligned) from the channel region" 103. On the contrary, such means that Fig. 1A's impurity regions 104 are preferably aligned with the channel region 103 along the source region 101, as evidenced by Yamazaki's Figs. 17A-17C disclosure.

The applicant's conclusion: "Since Yamazaki does not disclose the boundary between the channel region/source or drain region and the boundary between the impurity or [pinning] region/source or drain region as being aligned, there is nothing to teach or suggest that the combination would result in the floating gate overlapping a boundary between the source or drain regions and the [pinning] regions," is incorrect because its premise is incorrect. Again, Yamazaki does in fact disclose that the pinning regions and the channel regions are aligned along the source region. See Yamazaki's Figs. 17A-17C disclosure, for example.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner